Predicting Circuit Aging Using Ring Oscillators

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Introduction

- Predominant.
- Increases $V_{th}$, thus decreasing maximum frequency, $f_{Max}$ of circuits.
- Aging in PMOS by negative BTI, in NMOS by Positive BTI.
**Contribution**

- Predict circuit aging using delay degradation data of on-chip ring oscillators (ROSC).

- ROSC degradation measured by beat frequencies with respect to a reference ROSC [Lu (IBM), IRPS13].

- Infer delay degradation of circuit under test (CUT) from ROSC.
Why ROSC?

**Pros**
- Small and easily repeatable.
- Easy to lay out.
- Easy to measure $\Delta D_{ROSC}(t)$ using phase comparator as shown:

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[Kim, ISVLSI07]
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**Cons**
- Measuring ROSC is not equivalent to measuring CUT.
- Needs calibration to be used as aging sensor.
BTI aging

\[
\frac{\partial g}{\partial V_{th}} \bigg|_{V_{th}(t_0)} K h(\xi) \left( f(t) - f(t_0) \right) \Delta V_{th}(t)
\]

Thus, \( D(t) = D(t_0) + \frac{\partial g}{\partial V_{th}} \bigg|_{V_{th}(t_0)} K h(\xi) \left( f(t) - f(t_0) \right) \Delta V_{th}(t) \)

\( \Delta V_{th,n}(t) = K_1 h(\xi_1) f(t) \): Positive BTI

\( \Delta V_{th,p}(t) = K_2 h(\xi_2) f(t) \): Negative BTI

\( \xi_1 \) and \( \xi_2 \) are probabilities that the signal is high and low, respectively.

Fresh Device
\( D(t_0) = g(V_{th}(t_0)) \)

Degraded Device
\( D(t) = g(V_{th}(t)) \)
What is $f(t), c$?

- $f(t), c$ depend on aging mechanism:

**Reaction-Diffusion (RD) model**

$$\Delta V_{th}(t) = k_1 e^{E_0} \frac{-k_2}{e^{T/TT} t^n}$$

**Charge-Trapping (CT) model**

$$\Delta V_{th}(t) = k_3 e^{E_0} \frac{-k_4 V_{dd}}{T} \frac{k_5}{e^{T}} (A + \log(1 + Ct))$$

- Delay degradation from $t_0$ to $t$:

$$\Delta D(t) = k \left( f(t) - f(t_0) \right); \quad k = c \left. \frac{\partial g}{\partial V_{th}} \right|_{V_{th}(t_0)}$$

$k$: aging sensitivity, depends on $T, V_{dd}$ and $\zeta$. 

BTI aging of critical paths

Critical paths may change during lifetime.

CUT delay: piecewise smooth curve.

For CUT with four critical paths

Multiple critical paths crossover
For CUT with four critical paths

For ROSE with one path

Variable aging sensitivities

Constant aging sensitivity

CUT delay approximated by analytical bound, called the Upperbound on $f_{Max}$ (UofM) bound of delay.
**UofM bound of delay**

\[ D_{\text{CUT}}(t) = D_{\text{CUT}}(t_0) + k_{\text{CUT}} (f(t) - f(t_0)) \]

\[ k_{\text{CUT}} = \frac{D_{\text{CUT}}(t_f) - D_{\text{CUT}}(t_0)}{f(t_f) - f(t_0)} \]

\( D_{\text{CUT}}(t_0), D_{\text{CUT}}(t_f) \): by performing STA on CUT at \( t_0 \) and \( t_f \).

\( f(t_0), f(t_f) \): computed analytically; \( \zeta = 0.95 \) for both NBTI and PBTI.

**ROSC:**

\[ D_{\text{ROSC}}(t) = D_{\text{ROSC}}(t_0) + k_{\text{ROSC}} (f(t) - f(t_0)) \]
CUT delay degradation from ROSC

\[ \Delta D_{CUT}(t) = k_{CUT}(f(t) - f(t_0)); \Delta D_{ROSC}(t) = k_{ROSC}(f(t) - f(t_0)) \]

Features of \( D \):

- Independent of \( t, T \) and \( V_{dd} \).
- CUT with one dominant critical path: true \( \Delta D_{CUT}(t) \).
- CUT with multiple critical paths: pessimistic \( \Delta D_{CUT}(t) \).
Maximum pessimism in \textit{UofM} bound

- Generate CUT with two paths:
  - Path\(_1\) (\(C_{\text{bot}}(t)\)): gates with minimum aging sensitivity, \(k_1\)
  - Path\(_2\) (\(C_{\text{top}}(t)\)): gates with maximum aging sensitivity, \(k_2\)

- Adjust number of stages so that \(\Delta_1 = \Delta_2\) (see figure).

\[
E_{\text{max}} = \frac{(k_2 - k_1) \left( f(t_f) - f(t_0) \right)}{4}
\]

Maximum fractional error, depends on gate library

\[
E_{\text{frac}} = \frac{E_{\text{max}}}{C_{\text{top}}(t')} = \frac{4E_{\text{max}}}{d_1d_2 \left( \frac{k_2}{d_2} - \frac{k_1}{d_1} \right) \left( f(t_f) - f(t_0) \right)}
\]
Experimental setup

- RD Model of BTI aging: $f(t) = ct^{1/6}$
- Bound on maximum pessimism by $UofM$ bound ($E_{frac}$): 3.59%
- Lifespan of CUT: 10 years (beyond 3 months of burn-in)

**Gate functionalities**
- INV, BUF, 2 & 3-input NAND, NOR, 3 & 4-input AOI: each X1, X2 and X4

**Gate library**
- NanGate 45nm Open Cell Library

**Transistor model**
- 45nm Predictive Technology Model

**Benchmark circuits**
- ISCAS’89, ITC’99 synthesized in Synopsys Design Compiler

**Machine used**
- 64-bit Ubuntu server (Intel® Core™2 Duo CPU E8400 3GHz)
### Degradation ratio for various CUTs

<table>
<thead>
<tr>
<th>CUT</th>
<th>No. of gates</th>
<th>$D$</th>
<th>Error (%)</th>
<th>Runtime (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>s5378</td>
<td>690</td>
<td>1.51</td>
<td>0.17</td>
<td>0.50</td>
</tr>
<tr>
<td>s13207</td>
<td>590</td>
<td>1.88</td>
<td>0.00</td>
<td>0.46</td>
</tr>
<tr>
<td>s15850</td>
<td>336</td>
<td>1.95</td>
<td>0.00</td>
<td>0.36</td>
</tr>
<tr>
<td>s mult</td>
<td>1616</td>
<td>1.95</td>
<td>0.00</td>
<td>0.78</td>
</tr>
<tr>
<td>s38417</td>
<td>4565</td>
<td>2.79</td>
<td>0.09</td>
<td>1.75</td>
</tr>
<tr>
<td>s38584</td>
<td>4585</td>
<td>2.61</td>
<td>0.00</td>
<td>1.69</td>
</tr>
<tr>
<td>b15</td>
<td>6311</td>
<td>6.35</td>
<td>0.00</td>
<td>5.18</td>
</tr>
<tr>
<td>b17</td>
<td>17882</td>
<td>6.28</td>
<td>0.00</td>
<td>16.95</td>
</tr>
<tr>
<td>b18</td>
<td>67776</td>
<td>12.78</td>
<td>0.00</td>
<td>31.64</td>
</tr>
<tr>
<td>b19</td>
<td>128494</td>
<td>11.89</td>
<td>0.00</td>
<td>6.09</td>
</tr>
<tr>
<td>b21</td>
<td>24080</td>
<td>12.25</td>
<td>0.00</td>
<td>8.38</td>
</tr>
<tr>
<td>b22</td>
<td>36149</td>
<td>12.23</td>
<td>0.00</td>
<td></td>
</tr>
</tbody>
</table>

- **Practically, observed pessimism is negligible.**
- **Modest runtime: scalable to large CUTs.**
Temperature and $V_{dd}$ independence

$k_{CUT}$: dependent on $T$ and $V_{dd}$

$D$: independent of $T$ and $V_{dd}$

What about $D = \frac{k_{CUT}}{k_{ROSC}}$?

• Single $D$ for a CUT irrespective of operating conditions.
Conclusion

- BTI induced aging: signal probability dependent, captured by $U_{ofM}$ bound.

- On-chip ROSC as aging sensor:

- Degradation ratio, $\mathcal{D}$ transforms ROSC aging to CUT aging.

- Single constant predicts aging at all operating conditions.
THANK YOU